ESD-TR-75-351

MTR-3072

THE MULTI-MINICOMPUTER PROCESSOR

FEBRUARY 1976

Prepared for

DEPUTY FOR SURVEILLANCE AND NAVIGATION SYSTEMS
ELECTRONIC SYSTEMS DIVISION
AIR FORCE SYSTEMS COMMAND
UNITED STATES AIR FORCE
Hanscom Air Force Base, Bedford, Massachusetts

Project No. 6290
Prepared by
THE MITRE CORPORATION
Bedford, Massachusetts
Contract No. F19628-76-C-0001

REVIEW AND APPROVAL

This technical report has been reviewed and is approved for publication.

John E. Dunkle

JOHN E. DUNKLE, Major
Project Manager

James E. Troutman

JAMES E. TROUTMAN, 1Lt
Project Engineer

FOR THE COMMANDER

Roy F. Pollino

ROY F. POLLINO, GS-15
System Program Director
Weather Instrumentation SPO
Deputy for Surveillance and Navigation Systems

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Date Entered)*

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER ESD-TR-75-351	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE *(and Subtitle)* THE MULTI-MINICOMPUTER PROCESSOR		5. TYPE OF REPORT & PERIOD COVERED
		6. PERFORMING ORG. REPORT NUMBER MTR-3072
7. AUTHOR(s) D. D. Coffin H. E. T. Connell		8. CONTRACT OR GRANT NUMBER(s) F19628-76-C-0001
9. PERFORMING ORGANIZATION NAME AND ADDRESS The MITRE Corporation Box 208 Bedford, MA 01730		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS Project No. 6290
11. CONTROLLING OFFICE NAME AND ADDRESS Deputy for Surveillance and Navigation Systems Electronic Systems Division, AFSC Hanscom Air Force Base, Bedford, MA 01731		12. REPORT DATE FEBRUARY 1976 13. NUMBER OF PAGES 56
14. MONITORING AGENCY NAME & ADDRESS*(if different from Controlling Office)*		15. SECURITY CLASS. *(of this report)* UNCLASSIFIED 15e. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT *(of this Report)*

17. DISTRIBUTION STATEMENT *(of the abstract entered in Block 20, if different from Report)*

Approved for public release; distribution unlimited.

18. SUPPLEMENTARY NOTES

19. KEY WORDS *(Continue on reverse side if necessary and identify by block number)*

DIGITAL MTI
DISTRIBUTED PROCESSING
ELECTRO-OPTICS

20. ABSTRACT *(Continue on reverse side if necessary and identify by block number)*

The digital "snapshot" moving target indication (MTI) technique was developed for the GEODSS project in FY-75. GEODSS is a Ground-based Electro-Optical Deep Space Surveillance System.

This document describes the computer hardware used as a vehicle on which suitable real-time MTI implementation could be tested. The computer hardware consists of

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE *(When Date Entered)*

19. Key Words (Continued)

GEODSS Ground-Based Electro-Optical Deep Space Surveillance System
MINICOMPUTERS
MULTI-COMPUTER NETWORKS
MULTI-COMPUTER SOFTWARE
MULTI-MINICOMPUTERS
NETWORK SOFTWARE
NETWORKS
REAL-TIME PROCESSORS
SNAPSHOT MTI

20. Abstract (Continued)

ten interconnected Data General Corporation 800 series computers and their associated peripherals. This multi-minicomputer processor (MMCP) constitutes sufficient computing power to achieve an operational real-time MTI processor.

ACKNOWLEDGMENT

This report has been prepared by The MITRE Corporation under Project No. 6290. The contract is sponsored by the Electronic Systems Division, Air Force Systems Command, Hanscom Air Force Base, Massachusetts.

The use of the MCA bus as a communication medium has been a considerable advantage in building a flexible multicomputer system. Tom Dillman, formerly of the Data General Corporation, recognized the applicability of the bus approach to this multi-processor. We gratefully acknowledge his contribution.

TABLE OF CONTENTS

		Page
LIST OF ILLUSTRATIONS		5
LIST OF TABLES		5
GLOSSARY		6
1.0	INTRODUCTION	7
2.0	SYSTEM CONFIGURATION	9
2.1	The Computers	9
2.2	The MCA Bus	9
2.3	The Dual Ported Novadisc	12
2.4	The Inter-Processor Bus	17
2.5	Real Time Clock (Interval Timers)	17
2.6	Computer Peripherals	17
	2.6.1 Computer 1-PIM	17
	2.6.2 Computer 2-DIM	19
	2.6.3 Slave Computers - CAMs, TRKIN, Display RECM	20
3.0	SYSTEM ELEMENTS	23
3.1	PIM	23
3.2	DIM	23
3.3	CAMS	25
3.4	TRKIN	26
3.5	Display RECM	26
4.0	DATA GENERAL CORPORATION SYSTEM SOFTWARE	28
4.1	Real Time Disk Operating System	29
4.2	Extended Assembler	31
4.3	Text Editor	33
4.4	Extended Relocatable Loader	34
4.5	Octal Editor	35
4.6	File Management	35
5.0	SPECIAL INTERFACE	38
5.1	The Preprocessor Interface	38
5.2	The Display Interface	40
5.3	Miscellaneous System Input/Output	40
6.0	SYSTEM RELIABILITY	42
6.1	Life Test	42
6.2	Special Problems	45
7.0	SUMMARY AND CONCLUSIONS	48

TABLE OF CONTENTS (Continued)

		Page
APPENDIX I	DETAILED EQUIPMENT INVENTORY	51
REFERENCES		55
BIBLIOGRAPHY		57

LIST OF ILLUSTRATIONS

Figure Number		Page
1	Physical Assembly of MITRE MMCP	10
2	MITRE MTI MMCP System Configuration	14
3	Control and Data Paths for the PIM Interface	38

LIST OF TABLES

Table Number		Page
I	Characteristics of Nova 800 Series Computers in MITRE MMCP	11
II	Characteristics of Multiprocessor Communications Adapter (MCA)	13
III	Characteristics of Novadiscs	15
IV	Characteristics of Inter-Processor Bus (IPB)	18
V	Characteristics of Peripherals in MITRE MMCP	22
VI	Summary of Critical Rates	24
VII	Equipment List According to Delivery Dates	43
VIII	Equipment Failures During Life Test	44

GLOSSARY

CAM	Cancellation Minicomputer
CRT	Cathode Ray Tube
DGC	Data General Corporation
DIM	Disc Interface Minicomputer
DMA	Direct Memory Access Channel
GEODSS	Ground-based Electro-Optical Deep Space Surveillance System
GPIO	General Purpose Input Output board
IPB	Inter-Processor Bus
MCA	Multiprocessor Communications Adapter
MMCP	Multi-minicomputer Processor
MTI	Moving Target Indication
PIM	Preprocessor Interface Minicomputer
RDOS	Real Time Disk Operating System of DGC
RECM	Reconstruction Minicomputer
RLDR	Extended Relocatable Loader of DGC
TRKIN	Track Initiation Minicomputer

1.0 INTRODUCTION

The Moving Target Indication (MTI) Technique feasibility study was conducted at MITRE for the Ground-based Electro-Optical Deep Space Surveillance System (GEODSS) in FY 1975. An accompanying document, ESD-TR-75-352, describes the real-time software developed to evaluate the "snapshot" MTI feasibility. This document describes the computer hardware and general system software as it was used to effect the evaluation. The vehicle for implementing the "snapshot" MTI technique is the MITRE Multi-Minicomputer Processor (MMCP), a configuration of 10 Data General Corporation (DGC) 800 series computers and their peripherals.

The snapshot MTI technique is a digital computation method which can be used to discover a satellite that moves slowly through a field of stars. The GEODSS observation system employs a telescope to obtain precise visual images of portions of the night sky. The images are focused onto a light sensitive storage tube to enable a conversion of visual images to electronic images. The storage tube is systematically scanned by an electron beam to effect a read out of the tube. The electron beam current is compared to a threshold to determine the presence of image points on the storage tube. The X, Y coordinates of the electron beam on the storage tube along with

an indication of amplitude comprise the data representing each detection. A preprocessor conditions these detections to remove the multiple detections one obtains as the beam scans across a single "point" image. The entire group is simply replaced by a single representative point. The resulting picture is a "snapshot" of the telescope field of view and is the input to the MTI processor. A sequence of snapshots is similar to the individual frames of a motion picture. A time sequence of frames from the same field of view may be compared to detect the motion of a point image.

The "snapshot" MTI technique requires a flexible and reliable computing capability with a large real-time data processing throughput requirement. To realize this capability the processing task has been divided into subtasks which can be managed in the time available. The division has taken the form of a serial decomposition of tasks which are separable and a parallel decomposition of the fundamental data base where serial decomposition is inadequate.

The success of this task subdivision rests on the ability to distribute data to processing elements or computers with minimal overhead to the computers at each end of the data transfers. This efficiency of data transfer is achieved through the use of the Multiprocessor Communications Adaptor (MCA) which is a standard option from the Data General Corporation (DGC).

2.0 SYSTEM CONFIGURATION

2.1 The Computers

The MITRE MMCP is a configuration of ten DGC 800 series computers and peripherals. Figure 1 illustrates their physical assembly. Of the ten DGC Nova computers in the system, two are 800 Jumbo series computers with 24K 16-bit words of core, and eight are 820 series computers with 16K 16-bit words of core. The primary difference between the 800 and 820 series is in the ability of the computer power supply to accommodate the power drain of peripheral equipment. Each computer has 4 accumulators, an I/O system with programmed data transfer, a 16 level programmed priority interrupt, and a direct memory access (DMA) data channel. Full memory cycle time is 800 nanoseconds, and these computers execute arithmetic and logical instructions in a single cycle. Table I describes the characteristics of these computers in greater detail.

2.2 The MCA Bus

All 10 computers have the Multiprocessor Communications Adapter (MCA) option, which consists of a transmitter, a receiver and a common communications bus. This option is described as follows in How to Use the Nova Computers, a Data General Corporation publication:

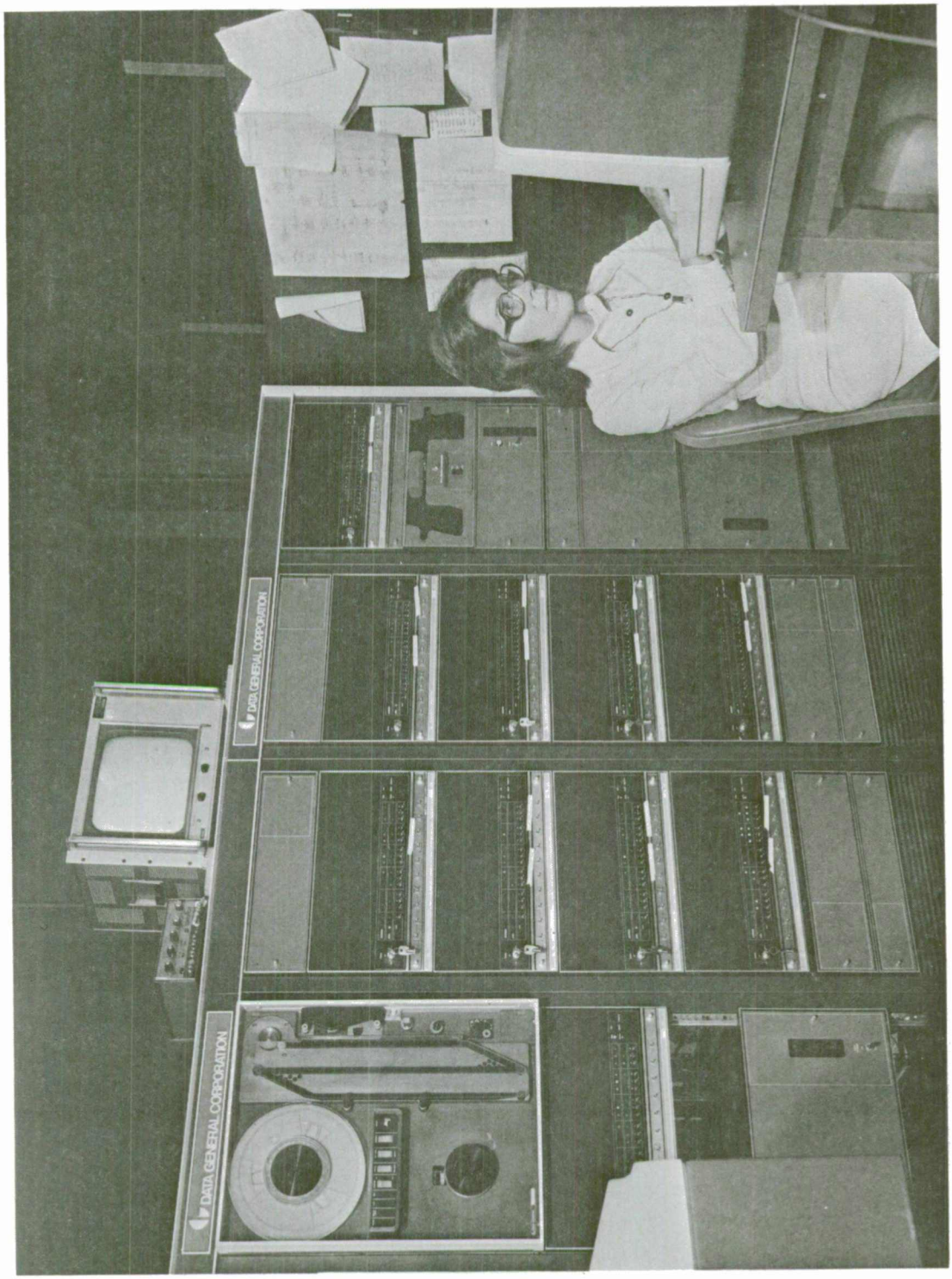

Figure 1 PHYSICAL ASSEMBLY OF MITRE MMCP

TABLE I

Characteristics of Nova 800 Series Computers in MITRE MMCP

	800 Jumbo (DGC Model 8238)	820 (DGC Model 8284)
Memory Size	24K words	16K words
Word Size	16 bits	same
Cycle Time	.8μ sec	same
Addressing		
.Direct	Present counter ±128 & Base page (256)	same
.Indirect	All core (adds 1 cycle)	same
.Indexed	Accumulator 2±128 Accumulator 3±128	same
. Auto Indexed	8 incrementing locations (20-27) 8 decrementing locations (30-37) adds 1/4 cycle	same
.Logical skip conditions	adds 1/4 cycle	
Memory reference	2 cycles	same
Add-subtract	1 cycle	same
Logical-register	1 cycle	same
Maskable Priority Interrupts	16 levels	same
Multiply/Divide	11 cycles	same
High Speed Data Channel I/O		
.Input	.8μ sec	same
.Output	.8/1.0μ sec	same
.Latency	<3.6μ sec	same
I/O Slots		
.Number Available	12	5
.DC Current Drain	24.9	8.9

> This option makes it possible to connect up to fifteen Nova-line computers into a multiprocessor system by permitting the transfer of blocks of data from one computer to another through their data channels. One adapter is attached to the IO Bus of each computer in the system, and the adapters are connected together by a common communication bus. Although mounted on a single circuit board, an adapter (MCA) is actually two independent interfaces, allowing simultaneous reception and transmission of data. Each interface is connected separately to the data channel, so the program need only set up an interface for receiving or sending and all transfers to and from memory are then handled automatically. To operate with the data channel, the receiver and transmitter each have an address counter and a word counter as well as data and status registers.[1]

The MCA bus is capable of 500 kilohertz bandwidth when limited to a total equivalent cable length of 50 feet. In this system the cable length exceeds 100 feet and therefore has a 300 kilohertz bandwidth. Table II gives an overview of the capabilities of MCA.

2.3 The Dual Ported Novadisc

Referencing the computers according to the numbering scheme in Figure 2, computers 1 and 2 are both 800 Jumbo series computers and both are connected to each disc. Each computer has 2 disc controllers, allowing it to access either disc or both. Each disc has dual ports, with one port serving as an access portal for each of the two computers. Table III provides more details on the Novadisc.

TABLE II

Characteristics of Multiprocessor Communications Adapter (MCA)

I/O Characteristics of MCA With Nova 800 Series Computers

- o 70 Kilowords per second maximum intercomputer transfer rate (unsynchronized)
- o 300 Kilowords per second maximum MCA loading by multi-computer exchanges
- o May connect up to 15 computers
- o Transmitter/receiver computer pair are run time reselectable
- o Block transfer with status available to transmitter and receiver

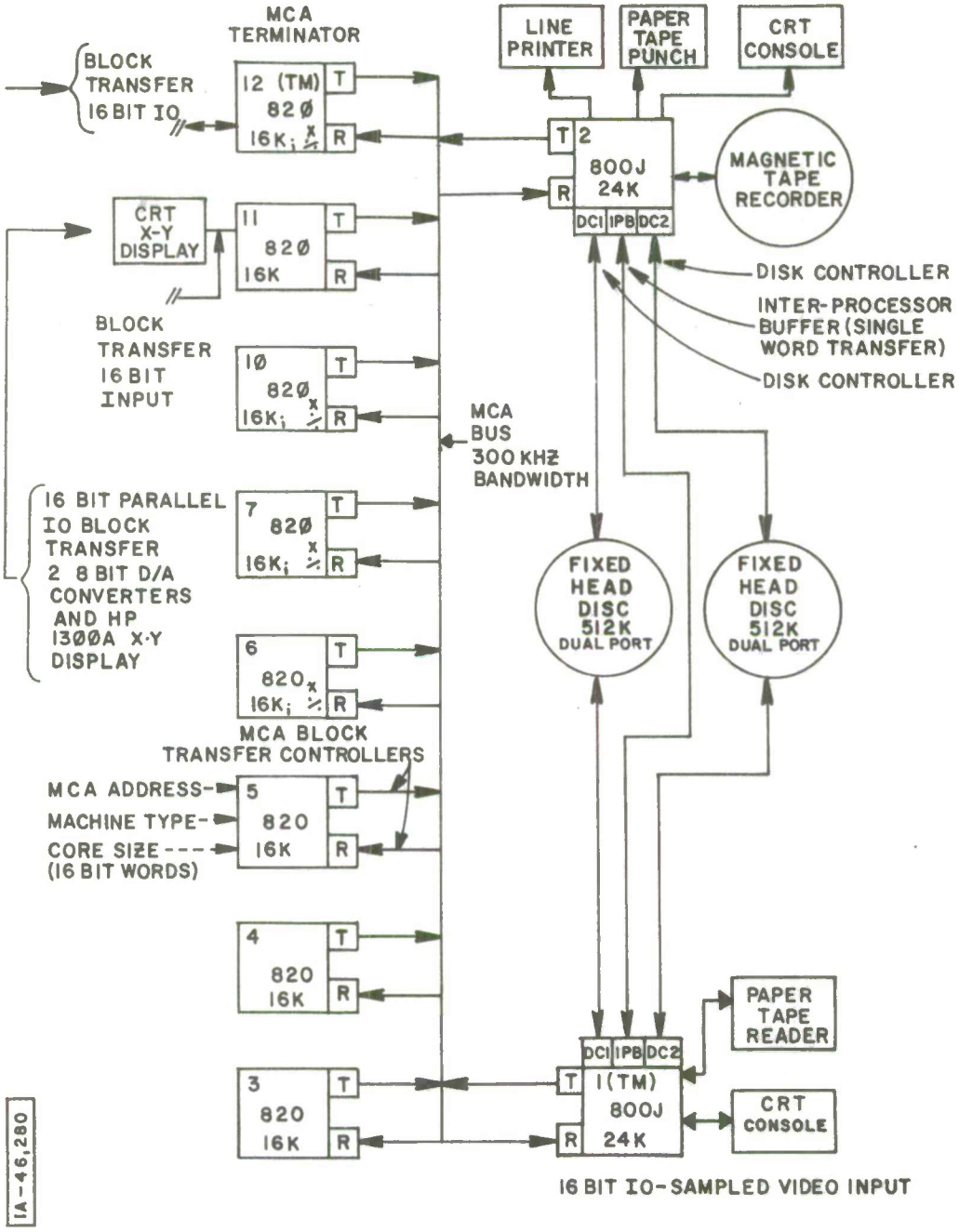

Figure 2. MITRE MTI MMCP SYSTEM CONFIGURATION

TABLE III

Characteristics of Novadiscs

Disc capacity	524,288 16-bit words
Transfer rate (Programmed with track/sector access optimized)	61,440 words per second
Dual Ports	Transfer directly (to/from) disc (from PIM to DIM)
Words per sector	256
Sectors per track	8
Number of tracks	256
Fixed head operation	
o Maximum latency	16 milliseconds
o Average latency	8 milliseconds

These interconnections allow for the use of the two discs as an alternating buffer for transfers or storage between the 800 Jumbos in the MTI software. The Inter-Processor Bus (IPB) adds one further path between the two Jumbos. With this additional connection, the 800 Jumbos, their peripherals and one selected or primary disc may be used to serve as a dual processor for software development. The Real Time Disk Operating System (RDOS) may be configured to use this system according to standard Data General Corporation procedures. RDOS, which is described elsewhere, is the manufacturer-supplied disc resident software system to enable easy use of perhipherals, efficient maintenance and filing of data and programs, and to serve as a system software manipulation tool.

RDOS permits the disc to be divided into partitions. The contents of partitions are described by directories. The disc allocation used in the MITRE system consists of two partitions, one for the storage of MTI system software and the other for RDOS system software. RDOS permits files, contents of a particular partition, or contents of the entire disc to be dumped to a magnetic tape recorder. Similarly, files from the magnetic tape recorder may be dumped to a particular area of the disc. The magnetic tape recorder must be addressed from computer 2.

2.4 The Inter-Processor Bus

The DGC Inter-Processor Bus (IPB), connects computers 1 and 2, for the special purpose of allowing them to transfer information between one another without using an intermediate storage device. The IPB's function of controlling two processors' access to a third device is especially applicable to the MITRE MMCP shared disc environment. Table IV lists the functions and special characteristics of the IPB.

2.5 Real Time Clock (Interval Timers)

Computers 1 and 2 have real-time clocks which generate a sequence of pulses to signal processor timing. Each clock frequency may be established for RDOS at the time of system generation. The clocks are used in RDOS or may be used in application programs for timing and control.

2.6 Computer Peripherals

This section associates the peripheral equipment with its resident computer. The intended use is also given for each computer which has special capabilities owing to its peripherals.

2.6.1 Computer 1 - PIM

Input/output devices connected to this computer are intended to reflect its role as the MTI system software data input portal and software development center.

TABLE IV

Characteristics of Inter-Processor Bus (IPB)

Functions of the IPB:

- o Transmits data over a half-duplex (interlocked) transmission line, allowing only one computer to transmit at a time. The transmission is under direct program control.
- o Transmits data over a full-duplex (non-interlocked) transmission line, allowing dual processor communication to be under direct program control.
- o Implements a watchdog timer with a timing period of 1 second which alerts each computer of a failure in the other.

Maximum transfer rate in dedicated routine	100,000 16-bit words per second
Single word transfer	

A high speed paper tape reader is used for the general input of off-line prepared punched tapes and for the general input of binary data in suitable formats. An Infoton Video Console is used for programmer/operator communication with RDOS, or any manually supplied text required by the PIM.

The preprocessor input is a general purpose 16-bit parallel transfer device which contains block transfer logic. The intended use of this device is to supply handshaking and a data portal for the MTI system input device. This device must be capable of computer cycle limited transfer rates.

2.6.2 Computer 2 - DIM

This computer, which similarly to computer 1 contains the disc access capacity, serves uniquely as the MTI processor disc interface element. That is, the operational use of this computer is restricted by design to be a means to retrieve data from a disc file.

The line printer and high speed punch are connected to this computer rather than to computer 1 to allow more freedom in their use in obtaining program listings and hard copies of software. They may be used with general disregard to other occurrences in the software development computer. An Infoton Video Console is also available primarily for RDOS communication, although other uses are possible.

A magnetic tape recorder is also connected to enable the logging of data, system errors and various outputs during testing of the MTI software in an operational environment. It is currently available to obtain backup copies of entire software systems and the RDOS system itself.

2.6.3 Slave Computers - CAMs, TRKIN, Display RECM

The remainder of the computers are all 820s and have 16K of core memory in comparison to the 24K core memory of the 800 Jumbos. All slaves (and masters) are connected to the MCA bus which serves as their data and software transfer channel. The only software development oriented feature of these computers is a teletype interface connection. A single teletype is available at MITRE and it may be fastened to any one computer for use in diagnostic tests. Occasional use was made of this feature also to obtain MTI printouts at intermediate stages of the process.

Four of these computers have also been equipped with the DGC hardware multiply/divide option. Computers in the MTI processing chain which require highly repetitive calculations may use these machines. Computers possessing this option are currently numbers 6, 7, 10 and 12.

One computer is capable of data output to a display through a parallel pair of 8-bit D/A converters. The converters may be run at variable sampling rates determined by an external timing source.

The timing is also used in the block control logic of the interface and thus controls the output, making it compatible with the sampling.

Tables V and VI summarize the characteristics of all peripherals and the critical rates of various I/O devices for this system configuration.

TABLE V

Characteristics of Peripherals in MITPE MMCP

Infoton video console	20-line, 80-character TTY compatible
Data Products line printer	300 lines per minute 136 columns, 64 character set
DGC High Speed Paper Tape Reader	400 Characters per second 8 channel, fanfold tape
DGC High Speed Paper Tape Punch	63.3 characters per second 8 channel, fanfold tape
DGC Magnetic Tape Recorder	75 inches per second 800 characters per inch 9 channel tape, industry compatible
Real time clock	4 frequencies: line, 10 Hz, 100 Hz, 1000 Hz

3.0 SYSTEM ELEMENTS

This section describes the role intended for each computer in order to perform the MTI function.

3.1 PIM

The role of the Preprocessor Input Minicomputer (PIM) is fulfilled by computer 1, as shown in Figure 2 and as described in Section 2.0. This computer has 24K 16-bit words of core and its intended use is to input large quantities of data. Currently data input is from the high speed paper tape reader and may consist of up to 5,000 x, y coordinate pairs. Eventually its input will be from the preprocessor via the digital input/output interface. The PIM will write the frames of data to the Novadisc fixed head discs, using the Inter-Processor Bus to communicate that data's frame number, scan number, and disc, track and sector address to the DIM, as well as the status of the PIM in using the disc.

The data taken in via the input medium is sent via the MCA bus in its original form (frame) to the DIM and display RECM. The CAMs receive portions of the frame from the PIM over the MCA bus. The transfers consist of a 16 word Header from the PIM followed by a 5 word Acknowledge from the appropriate computer. An Acknowledge may be followed by a large data block or another Header depending on software logic.

3.2 DIM

TABLE VI

Summary of Critical Rates

Clear channel DMA	In 1250 kilowords per second Out 1000 kilowords per second
MCA I/O between minicomputers	70 kilowords per second
MCA maximum loading	300 kilowords per second
Disc I/O (Optimized mode)	61.4 kilowords per second

Computer 2 and its peripherals, shown in Figure 2 and described in Section 2.0, are designed for use as the Disc Interface Minicomputer (DIM). In an operational software environment while performing its MTI role the DIM will accept descriptions of the data arriving at the PIM from the preprocessor. The messages are sent by the PIM over the IPB and will include disc filing information. The DIM will then use these data to retrieve the appropriate corresponding frame from its place in the disc file. The data retrieved from the disc will be thresholded and sorted for distribution to the CAMs. The Header, Acknowledge and Data block sequence is required for transfer as for the PIM.

In the current software the DIM receives large blocks of x, y coordinate pair data from the PIM via the MCA bus, along with appropriate headers and reset headers. It also utilizes the MCA bus to send acknowledge blocks to the PIM and the CAMs, as well as to send the sorted PIM data with a threshold applied for cancellation.

3.3 CAMS

Computers assigned for cancellation may be any four from the series 3 through 10 or 12 as shown in Figure 2 and described in Section 2.0. Each CAM receives header blocks and data blocks from the DIM and the PIM via the MCA bus during each MTI cycle. It transmits acknowledge blocks via the MCA bus to the DIM and PIM upon receipt of a header. Each CAM also transmits via the MCA bus header blocks

and data blocks consisting of leaker data resulting from the cancellation of the DIM and PIM data to the Track Initiation machine (TRKIN) and to the display Reconstruction Minicomputer (display RECM).

3.4 TRKIN

Any remaining computer described in Section 2.0 and shown in Figure 2, except number 11 which has display capabilities, may be used for the track initiation function (TPKIN). Only one computer is required for TRKIN in the MITRE Multi-Minicomputer Processor at present. TRKIN receives reset headers from the PIM via the MCA bus as well as headers and leaker data from the four CAMs. It transmits an acknowledge via the MCA bus for each header block that it receives from a CAM. When TPKIN has examined frames of leaker data for potential tracks, it transmits via the MCA bus this list of tracks along with an appropriate header to the display RECM.

3.5 Display RECM

Computer 11 and its peripherals, shown in Figure 2 and described in Section 2.0, are designed for the display Reconstruction Minicomputer (display RECM). This computer receives headers and data blocks from the PIM, the 4 CAMs, and TRKIN, and displays this data on an HP1300A x, y display. It uses a standard IO interface card connected to two D/A converters with the display. The timing is supplied externally. Each x 16-bit word is truncated to 8 bits and

placed in the lower 8 bits of the display word. The words are presented to the D/A converter pair as dictated by the external timing source. Analog output is then presented to the deflection plates of a CRT. No blanking is currently used. The apparent persistence supplied by the digital nature of the analog output is adequate for the purposes intended.

The context of the display is arbitrary and is determined by computer program logic. Current contents include the option of star field, leaker field or track field where field is defined to be an x, y presentation of data values.

4.0 DATA GENERAL CORPORATION SYSTEM SOFTWARE

A complete set of Data General Corporation system software accompanies the MITRE Multi-Minicomputer Processor. The main element of the system software is the Real Time Disk Operating System (RDOS). It coordinates the use of the other disc resident system software, such as the Extended Assembler, with the user files stored on the disc. The file management capabilities of RDOS aid the user in creating, maintaining, and deleting his files and dumping them to an output device. Other elements of DGC system software used to develop the MITRE MTI system software were the Extended Assembler, the Text Editor, the Extended Relocatable Loader and the Octal Editor. Abstracts of these software elements follow, in order to give an overview of their uses and capabilities.

Software development on the MITRE Multi-Minicomputer Processor has been accomplished by using computers 1 and 2, as shown in Figure 2. These two computers together with the primary disc were employed as a dual processor system. Computer 1 is interfaced with an Infoton video display and a DGC high speed paper tape reader; and computer 2 is interfaced with another Infoton video display, a Data Products line printer, a DGC magnetic tape recorder and a DGC high speed paper tape punch. The user may interface with RDOS by utilizing Command Line Interpreter commands entered on the system console to load a source file, edit the file with the DGC Text Editor and assemble it via the DGC Extended Assembler. The assembled relocatable

binary output may be converted to a core image executable save file. Previously generated relocatable binary files may also be accessed with the DGC Relocatable Loader in the creation of save files. These files--source, relocatable binary and core image--may be copied onto either magnetic tape or paper tape. One may also obtain source listings on the line printer.

4.1 Real Time Disk Operating System

The MITRE MMCP is established with DGC RDOS, Revision 3.02. RDOS is modular in structure, and can be used with any Nova-line computer having 16K memory or more, any grouping of fixed or moving head disks and a console for input/output. [2]

As stated in Data General Corporation's User's Manual RDOS Real Time Disk Operating System:

> Some of the major features of RDOS are:
> - .Operating system is partly core-resident, partly disk-resident.
> - .Modular multitask monitor.
> - .Up to 128 overlay areas per user program.
> - .Spooling (disk buffering) of output.
> - .Buffered and non-buffered I/O.
> - .Support for real time FORTRAN IV and real time FORTRAN 5.
> - .Flexible file structuring.
> - .Hardware protected foreground/background operation.
> - .Dual and multiple CPU systems, with MCA communications support.
> - .Batch mode processing of user jobs.
> - .Disk partitioning and sharing of user files.
>
> RDOS provides all the comprehensive file system capabilities normally available on disk operating systems, allowing the user to edit, assemble, execute, debug, compile, load-and-go, save and delete files. Complete file protection is provided using a number of system defined attributes. File directories

are maintained on a fixed head disk and disk pack basis where each disk pack can be removed from the system. All peripheral devices are named and treated as files, providing complete device independence by symbolic name. Disk files may be organized sequentially, randomly, and contiguously.

Single task real time programs are supported, and RDOS can be loaded in modular fashion to run a full multitask program with all RDOS options within a minimum of 16K resident core storage. To permit the use of an RDOS system with minimal core storage, only those task processing modules required by the user programs are loaded from the system library. Moreover, RDOS system modules are segmented into system overlays to further optimize the use of core storage.

Multitask environments may include tasks with a hierarchy of up to 256 classes of priority. There is no limit to the number of tasks within each priority class, and all tasks are assigned a relative priority within each class. Tasks may be synchronized by communicating with one another, or they may compete for CPU control asynchronously in a real time environment.

Systems with a real time clock maintain a system clock and calendar for scheduling task activities on a time-of-day basis. Tasks may obtain or set the correct time in seconds, minutes, hours, or the day of the year. Tasks may also synchronize their activities with the real time clock for periods as short as one millisecond each. A new Task-Operator Communications package, OPCOM, permits users at the console to examine and modify the status of tasks which are part of a program running in the foreground or background. The system clock and calendar are also used to record file usage information and BATCH mode job utilization of system resources.

Program tasks may exist within either resident multi-node root programs or program overlays. Each set of root program and all its associated overlays constitutes a program level, and up to five distinct program levels are permitted. Program chaining permits a single program to be segmented into distinct, sequential portions all effectively on a single program level. This feature permits the writing of programs whose total size far exceeds available core storage. Programs on different levels may either communicate by means of common disk files, or--in the case of FORTRAN programs--through blank common. The Command Line Interpreter (CLI) normally exists at the highest level, level zero, giving four remaining levels which are available for user programs.

> To increase system utilization, RDOS permits dual programming; that is, RDOS permits several, possibly unrelated functions to be performed concurrently and to share the basic system resources. The two programs which are allowed to run together under an RDOS dual programming system are a foreground and background program. Priority for CPU processing time is allocated to programs by RDOS, which may either give all foreground tasks priority over all background tasks or allocate system resources equally between the foreground and background.[2]

While the MITRE MMCP does not use RDOS during the MTI software operation, it is used 1) in developing the software, 2) in maintaining software files 3) in any non real-time communications between the disc and the magnetic tape recorder, line printer, punch, paper tape reader and consoles, and 4) in distributing software to other computers and achieving MTI system software startup. RDOS also allows the user to generate any number of unique operating systems, to store these systems on magnetic or paper tape, and to load them to the disc as desired. RDOS has proven to be a powerful tool in the MITRE MTI software development.

4.2 Extended Assembler

The DGC Extended Assembler processes a source file, which is written in assembly language by 1) converting it to machine language code, 2) producing an error listing on the first pass through the source file if any errors exist, 3) producing a source program listing which also includes the errors (optional), and 4) producing a relocatable binary file (optional). The relocatable binary file is an object file that can be loaded by the relocatable loader to generate an executable program.

The Extended Assembler provides basic assembly functions, as well as three special facilities. First, it provides two pseudo-ops ("permanent symbols that direct the assembly process" [3]) that indicate that a program's code is relocatable; otherwise by default the code is absolute. These pseudo-ops are .ZREL, used to indicate that all the code which follows is zero page relocatable code, and .NREL, used to indicate that all the code which follows is normally relocatable. This facility allows the Relocatable Loader to adjust the addresses of all the relocatable binary object files. Thus a program's loaded origin may be different from its assembled origin. Second, the Extended Assembler allows interprogram communication among programs assembled separately. As described in DGC's Extended Asembler User's Manual:

> Using the interprogram communication pseudo-ops, the programmer can:
>
> 1. Reserve a labelled or unlabelled program area to be shared by several programs (.COMM and .CSIZ),
> 2. Define entry symbols that can be referenced by other programs (.ENT), and
> 3. Name a program that is to become an overlay segemnt (.ENTO).[3]

Third, the Extended Assembler's conditional assembly facilities allow the user to include or skip sections of code during the assembly process.

Further details of the DGC Extended Assembler's operation may be obtained in DGC's Extended Assembler User's Manual.

4.3 Text Editor

The DGC Text Editor is used to create, modify, and update files of ASCII characters (i.e., source files) which are stored on the disc. The Text Editor is called via RDOS, and the files which it creates are compatible with RDOS.

As stated in the DGC Text Editor User's Manual:

> The commands used in the Editor are divided into groups, those that input and output the contents of the edit buffer and those that modify the contents of the buffer. The edit buffer is an area of memory in which input is stored while being modified. Input commands bring the text into the buffer, modification commands are used to change the contents of the buffer, and output commands transfer the updated files to the output device.
>
> The command structure is versatile enough to allow the modification of a single character, several characters, or a whole line. [4]

In developing the software for the MITRE MMCP the window mode has been found to be especially useful. At the start of the edit process, the window size is set equal to 59 lines, the number of lines on a page of source text. Whenever a Text Editor page is read into the edit buffer, exactly 59 lines will enter, corresponding to a page of the user's current listing. After this section of code is modified, the buffer, whatever its new size, is output to the new file. Then the next page of 59 lines is read in and the process continues. This feature of the Text Editor makes working with large source files less cumbersome and keeps the edit buffer in core to a reasonable size.

The configuration of computers 1 and 2 are suitable for using the Text Editor, as they both share the primary Novadisc on which the DGC and MITRE MTI software reside. Each computer has a video display for communicating with RDOS and the Text Editor.

4.4 Extended Relocatable Loader

The DGC extended Relocatable Loader (RLDR) is used to resolve the individual relocatable binary files and system library files directed to it and to produce an executable core image save file, which is stored on the disc. The RLDR program is called by RDOS when RDOS receives a RLDR command naming all the binary files to be resolved.

As stated in DGC's Extended Relocatable Loaders User's Manual:

> In relocatable assembly, storage words are assigned a relative location counter value. The value is initially zero and is incremented for every storage word generated. At the termination of assembly, if n words are generated, they are assigned to relative locations 0, 1 ....n-1. The actual addresses assigned to words generated are determined by the relocatable loader.
>
> The loader maintains the value of the first location available for loading, based on the programs previously loaded. As each assembled program is loaded, the relocatable loader updates the value of the first location available for loading. In this way, any number of separately assembled modules can be loaded together without any conflict in absolute storage assignment.
>
> Library files are simply collections of relocatable binary programs, one or more of which will be loaded to resolve external references appearing in previously loaded programs. [5]

When the RLDR command is given under RDOS, the Extended Relocatable Loader loads the relocatable binaries, absolute binaries, and library files in the same order as their names appear in the RLDR command line.

A listing of the core map, showing where each binary or library file begins, may be sent to either the video console or the line printer. The resulting executable file is a save file, which is stored on the disc in the format filename.SV. The save file may be recalled into the computer for execution at any time by relatively simple RDOS commands which do not use RLDR.

4.5 Octal Editor

The DGC Octal Editor allows the user to examine and modify any unprotected location in a disc file. The Octal Editor along with the name of the file to be examined is called via RDOS. The examination is done in octal, unless decimal or ASCII modes are specified.

The Octal Editor has been used for modifying save files for their use with the RDOS bootstrap program, MCABOOT, as well as for making temporary changes to save files during the debugging process.

4.6 File Management

RDOS considers a file to be any set of information, such as a source file, a relocatable binary file, a listing file, or a core image save file, or any device giving or receiving the information, such as a video console, a paper tape reader, a paper tape punch, a magnetic tape recorder or a line printer.

Each file has a unique name of up to 10 characters which may be upper case alphabetics, numerals, or $. I/O devices have certain

assigned file names, many of which start with a $, such as $TTO for teletype output. Each file also has file attributes, which are changeable by the user, and file characteristics, which are not changeable. Attributes pertain to certain features of files, such as their protectibility and type. Characteristics pertain to file organization and serve to identify special files, such as partitions, directories, and link entries.

RDOS permits the division of disc space via partitions, both primary and secondary, and subdirectories. The primary partition is all the disc space available after system generation. Fixed size subsets, called secondary partitions, amy be allocated by the primary partition. Sub-directories are variable size subsets of file space; within a primary or secondary partition their size increases or decreases depending on the space available to the parent partition. Information about the files within a partition or sub-directory is kept by a system file directory. Link entries in RDOS allow the user to access disc files or magnetic tape files outside of their current directory. This option allows system software, such as the Extended Assembler, to be placed in one partition and to be accessed by other subdirectories and partitions, thus saving large amounts of disc space.

In the MITRE MMCP one primary partition exists, in which all DGC system software and the system save and overlay files reside.

Two subdirectories have been established, one for MITRE software and one for DGC and user written diagnostic programs.

Through RDOS, files in a particular subdirectory or partition may be listed; disc space allocations may be determined; individual files or groups may be written to an output device; or individual files may be deleted. The details on file management are contained in DGC's User's Manual RDOS Real Time Disk Operating System.

5.0 SPECIAL INTERFACES

This section describes the MTI system input and output channels of the MMCP. There are three digital ports to the MMCP with each in a different computer. The uses of these ports are: 1) to establish an input channel from the preprocessor; 2) to provide a display window for the monitoring of intermediate results; 3) to provide an output route for MTI target information; and 4) to provide for inputs to the MMCP from other computers. All of these input/output channels are provided using the DGC General Purpose I/O interface board which includes block transfer, data channel, and busy-done logic necessary to effect high speed data block transfer.

5.1 The Preprocessor Interface

The interface between a preprocessor and the MMCP is shown in Figure 3. Control is achieved by the CLEAR, START, DATA FLAG, and DATA ACK pulses. The computer program may initiate the transfer by resetting the preprocessor. This is done with the CLEAR signal which results from the voluntary execution of a clear instruction addressing the GPIO card. The GPIO card has been assigned an address of 26_8. It has been assumed that the preprocessor will have its own natural reset cycle that is scheduled to occur at the beginning of each data acquisition cycle. The computer generated CLEAR will be used to indicate compatible timing; that is, should the preprocessor begin its cycle before the CLEAR arrives, then an error condition exists.

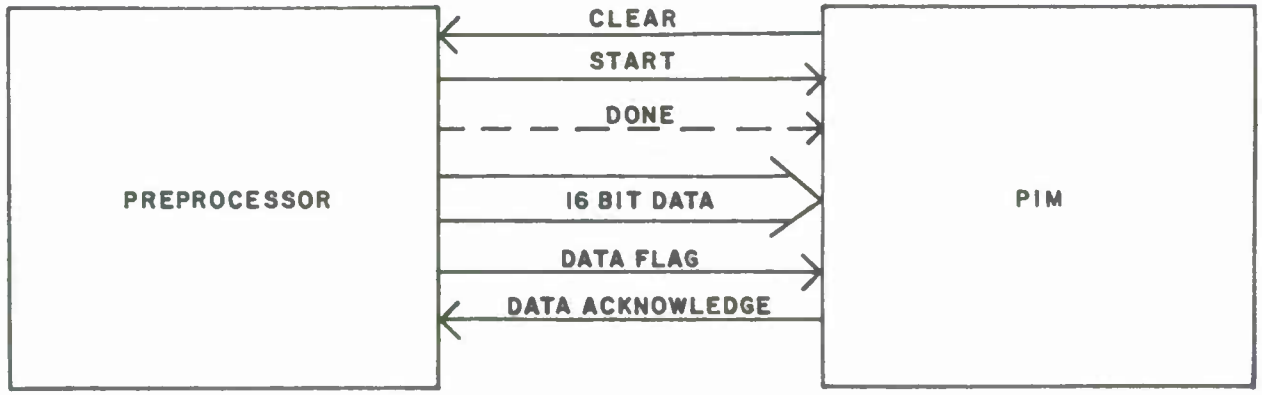

Figure 3 CONTROL AND DATA PATHS FOR THE PIM INTERFACE

5.2 The Display Interface

A GPIO board has been connected to one 820 series computer in order to provide a real-time x, y display of the data field. The interface block transfer hardware may be started by using the DGC conventions for the word count and address registers and the associated busy/done logic. The GPIO control then presents a block of binary computer half words to each axis of an x, y analog CRT display in sequence. Each half word is routed to an 8-bit D/A converter. Each D/A converter output then is routed to the proper deflection plate of the CRT.

The computer transfers are in response to a steady series of DATA ACKNOWLEDGE signals which are currently obtained from a standard pulse generator. The timing pulse rate is switch selectable from 0 to 1.25 MHz.

The D/A converters and associated logic are contained on a sub rack mounted in one of the MMCP equipment racks.

5.3 Miscellaneous System Input/Output

A third GPIO interface card exists for subsequent use in a real-time environment. This card will be used to input telescope position, time, and the coordinates of registration star data. It will also be used to output target information. This card has not been configured for specific input and output equipment as yet, since no specific data for the required interface has been available during this system's use in the feasibility study.

The START and DATA FLAG accompany each data word from the preprocessor in order to supply control logic timing and a window for stable data lines respectively. The START is used to obtain computer data channel access and manipulate block transfer logic; the DATA FLAG is a short pulse which indiates that the data lines have been set and may be read into the GPIO data register.

DATA ACK is the response by the GPIO card to signal the preprocessor that the interface is ready for the next data word. This may be used in the preprocessor to step to its next transfer cycle.

The GPIO card logic sets a DONE flip flop at the completion of its word count. The word count is a register that is initially set by the computer and stepped by each transfer. On reaching zero, the word count register sets DONE. Logic to enable the preprocessor also to set DONE directly is necessary to indicate the end of a data frame, but this has not been installed as yet.

There are 16 data lines which may used to convey data words as they become available. At this writing 12 data lines are connected. These 12 were used in a prototype preprocessor.

The GPIO card as currently designed is capable of transfers at a 1,250 kHz word transfer rate. This means that the timing has been arranged so as to enable the data transfers to access the computer on every memory write cycle.

6.0 SYSTEM RELIABILITY

The equipment in the MITRE MMCP was received in two major shipments, as shown in Table VII. The first group of equipment which arrived in late October, 1974 consisted of the basic components needed to implement the MITRE MTI technique. The second group of equipment which arrived in early February, 1975 consisted of software development equipment, another computer and another disc. This section will discuss the life tests which have been run on the equipment and the problems which have been encountered.

6.1 Life Test

Since the arrival of the first group of equipment, the computers and the primary Novadisc have been run 24-hours per day, 7 days per week with the exception of the times when equipment failed and repair was necessary. The other peripherals have been tested thoroughly with diagnostics being run as needed and equipment repaired as necessary. The specific failures experienced during the life test are outlined in Table VIII, with special problems summarized in Section 6.2.

In the early stages of the MMCP while MITRE MTI software was being developed and debugged, the diagnostic test program EXERCISEP was run whenever a machine had no specific function. This diagnostic performs the most thorough computer test for a single machine. Once the hardware multiply/divide option was added to machines 6,7,10 and 12, as shown in Figure 2, the Nova 800/1200 Multiply/Divide test

TABLE VII

Equipment List According to Delivery Dates

Equipment	Delivery Date
2 800 Jumbo Nova Computers, 24K, each with IPB, Disc Controller	October, 1974
1 Fixed Head Novadisc 512K, dual port	October, 1974
1 DGC Paper Tape Reader	October, 1974
1 Infoton Video Console	October 1974
7 820 Nova Computers, 16K	October 1974
9 MCA boards, 1 in each computer plus cable connecting all computers	October, 1974
1 820 Nova computer, 16K	February, 1975
1 DGC Paper Tape Punch	February, 1975
1 Infoton Video Console	February, 1975
1 Data Products Line Printer	February, 1975
1 DGC Magnetic Tape Recorder	February, 1975
1 Fixed Head Novadisc, 512K dual port	February, 1975
2 Disc Controllers, for computers 1 and 2	February, 1975
1 MCA Board plus cable	February, 1975

TABLE VIII

Equipment Failures During Life Test

Equipment Type	Cause of Failure	Date
1) Infoton Video Display	Burned resistor	11/22/74
2) MCA board in computer 3	Bad integrated circuit	12/3/74
3) Primary Novadisc	Damaged disc platter	1/22/75
4) MCA board in computer 6	Bad integrated circuit	2/20/75
5) Disc controller in computer 1	Damaged wires	2/21/75
6) Primary Novadisc	Damaged motor, start capacitor, relay and broken fan	2/24/75
7) MCA Cannon Connector on computer 1	Bad crimp connectors at common plug	3/19/75
8) Paper tape punch	Teeth on punch not properly set	4/11/75
9) Primary Novadisc	Burned resistor in start relay	5/28/75
10) Primary Novadisc	Cracked fan	6/11/75

was run alternately with EXERCISER whenever one of those machines was free.

After the MITRE MTI software was able to process frames of data, it was allowed to run for periods of time in its cycling mode, i.e., processing the same frame of data repeatedly. This aspect of life testing heavily exercised the MCA bus and led to the discovery of a design problem which involves the activation of the transmitter time-out function. This problem with the MCA and its temporary solution are discussed in detail in Section 6.2. Since DGC is actively seeking a permanent solution to the problem, it is not expected that another multiprocessor system would experience these difficulties in the future.

Since the application of the temporary fix to the MCA bus, the MITRE MTI software has run in its cycling mode for 200 hours before being voluntarily stopped by MITRE personnel. The life test has successfully exercised the equipment and served as a monitor, allowing problems to be detected in a timely manner.

6.2 Special Problems

This section will deal with the special problems related to failures of the primary Novadisc stated in Table VIII as well as the previously mentioned MCA problem.

The primary Novadisc required the most repairs of any piece of equipment in the system. Replaced were its disc pack, thermal switch,

start capacitor, motor, relay, and two fans. It also required controller connector rewiring due to an overheating problem. This problem was finally solved by physically moving computer 1, to which this controller was interfaced, further away from the primary Novadisc to allow better air circulation around the computer.

The problem with the MCA bus had been evident as soon as the MITRE MTI software was run in a cycling mode, but it became more acute with the addition of the tenth computer to the system in February, 1975. After extensive testing by MITRE and DGC personnel the system was modified by adding coaxial cable for control signals throughout the MCA bus. Also, termination resistors and load resistors on the MCA boards were changed to reduce reflections and noise on the MCA bus. An MCA design problem was discovered in the activation of the transmitter time-out function. It was grounded in order to avoid the timing problem.

This timing problem occasionally occurred when one word of a transfer finally gained access to a receiver after the source (transmitter) had been locked out for some time exactly matching the time-out interval. It was possible for the transmitter to time out in spite of the successful transfer, thus resulting in an illegitimate condition. The temporary solution has been to disengage the time-out function in all transmitters. The Engineering Department of DGC is working on a permanent solution to the problem.

Aside from these special problems with the primary Novadisc and the MCA bus, most problems have been due to failures which might reasonably be expected of equipment running during a shakedown period and then for many months on a 24-hour per day basis with all components operational.

7.0 SUMMARY AND CONCLUSIONS

The MMCP system was acquired in October of 1974. Delivery and initial shakedown were followed by a two-month period of familiarization with the equipment and a honing of programmer use of the MMCP and its software. This period was also used to help solidify the overall inter computer software structure.

With this background, a two-month period of program design and implementation was adequate to construct an operating MTI software system with some of the more critical functions completed. This development was severely hampered by a lack of a suitable set of software development peripherals. It should be noted that this difficulty was forseen but could not be avoided because of budgetary constraints.

The installation of the remainder of the equipment required one full month due to problems which were not forseen, namely, the MCA bus logic problem which has been currently bypassed but not solved by the manufacturer.

Subsequent software development has been rapid with the benefit of the added peripherals.

The manufacturer and the applications programmers at MITRE were not familiar with the sort of computer arrangement represented by the MMCP. This caused an initial period of necessary education; however, familiarity has led to a growing confidence in the extreme

power and flexibility of the MMCP. Any original misgivings related to the difficult programmming which was anticipated dissolved and the present sentiment is quite to the contrary in this regard.

Although Section 6.0 describes what seems to be a large list of problems, these are primarily related to the novelty of the MMCP to the manufacturer and the extensive installation of new equipment in the field. Operational experience beyond the installation period has left the impression that the normal use of hardware results in reliable performance as shown by the maintenance record beyond February.

The only recommendation which can be made for any future system of this sort is that computers should be made interchangeable wherever reasonable. Some system elements will benefit from their expanded capacity, while others will serve as a buffer capable of absorbing MTI system design changes. The MMCP will also become more flexible in accomodating other MTI approaches. A slightly larger initial system cost will be balanced by the reduced requirement for a stock of replacement parts and by simplified maintenance and operation.

APPENDIX I

Detailed Equipment Inventory

DGC Model Number	Description	Quantities as related to each computer									
		1	2	3	4	5	6	7	10	11	12
8238	Nova 800 Jumbo Computer with 24K core memory	1	1								
8284	Nova 820 computer with 16K core memory			1	1	1	1	1	1	1	1
4008	Real Time Clock	1	1								
8208	Automatic Program Load	1	1								1
8207	Hardware Multiply/Divide						1	1	1		1
4007	I/O Interface Subassembly	1	1	1	1	1	1	1	1	1	1
4010	Teletype I/O Interface	1	1	1	1	1	1	1	1	1	1
4010I	Infoton Video Display Console	1	1								
4023	Voltage (EIA-type) I/O Interface for 4010I	1	1								
4038	Multiprocessor Communications Adapter (MCA)	1	1	1	1	1	1	1	1	1	1

APPENDIX I (Continued)

Detailed Equipment Inventory

DGC Model Number	Description	Quantities as related to each computer									
		1	2	3	4	5	6	7	10	11	12
4039BA	MCA Cable	1									
4039AB	MCA Cable		1								
4039BB	MCA Cable			1	1	1	1	1	1		
4039F	MCA Cable										1
4190	General Purpose Interface Board (GPIO)	1								1	
4041	16-bit input and output register for 4190 GPIO board	1								1	
4042	Data channel connection for 4190 GPIO board	1								1	
4044	Wirewrap pins and 65 16-pin low profile sockets for dual in-line integrated circuits for GPIO board. (Intended use for MTI system I/O to Site Computer	1									

APPENDIX I (Continued)

Detailed Equipment Inventory

DGC Model Number	Description	Quantities as related to each computer									
		1	2	3	4	5	6	7	10	11	12
4011	Paper Tape Reader Control	1	1								
6013	High Speed Paper Tape Reader	1									
4012	Paper Tape Punch Control		1								
4012A	High Speed Paper Tape Punch		1								
4014	I/O Interface Subassembly for line printer		1								
4034	Line Printer Control		1								
4034G	Data Products Line Printer		1								
4034I	Line Printer Paper Stacker		1								
6021	Magnetic Tape System		1								
4019	Disc Controller for fixed head disc drives	2	2								
6003	Novadisc Fixed Head Disc (FHD) (2 total)	2	2								

APPENDIX I (Concluded)

Detailed Equipment Inventory

DGC Model Number	Description	Quantities as related to each computer									
		1	2	3	4	5	6	7	10	11	12
1035E	FHD Cable (2 total)	2	2								
4240	Inter-Processor Bus unit (IPB)	1	1								
1065A	IPB Cable (1 total)	1	1								

REFERENCES

1. Data General Corporation, How to Use the Nova Computers, DG NM-6, Southboro, Mass. October, 1972, 7:10.

2. Data General Corporation, User's Manual RDOS Real Time Disk Operating System, 093-000075-05, Southboro, Mass., April, 1974, i-ii.

3. Data General Corporation, Extended Assembler User's Manual, 093-000040-01, Southboro, Mass., May, 1974, 6:1, 6:17.

4. Data General Corporation, Text Editor User's Manual, 093-000018-07, Southboro, Mass., June, 1974, i.

5. Data General Corporation, Extended Relocatable Loaders User's Manual, 093-000080-02, Southboro, Mass., November, 1973, i.

BIBLIOGRAPHY

Data General Corporation, Octal Editor, 093-000084-00, Southboro, Mass., April, 1973.

Data General Corporation, Technical Reference 4240 Inter-Processor Bus, 014-000056-00, July, 1974.

The MITRE Corporation, MTI Processor Software, ESD-TR-75-350. Electronic Systems Division, Air Force Systems Command, Hanscom AFB, Bedford, Mass., February 1976.